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| EXAMINER | |
|---|---|
| VO, THANH DUC | |
| **ART UNIT** | **PAPER NUMBER** |
| 2189 | |

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/775,614 | SMITH ET AL. | |
| | Examiner | Art Unit | |
| | Thanh D. Vo | 2189 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☒ Claim(s) *25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/10/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is responsive to the Application filed on February 10, 2004. Claims 1-26 are presented for examination. The IDS filed on March 10, 2005 has been considered. Claims 1-26 are pending.

### *Drawings*

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

3. Claims 3, 6, 16, and 24 is objected to because of the following informalities:

As per claim 3, the term "complete" in line 2 should be – completed.

As per claims 6 and 24, the term "comprise" should be – comprises.

As per claim 16, the term "the first shift register" in line 2 should be – the address shift register; and "the second shift register" in line 2 should be – the data shift register.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "register bank" in lines 2-3 is not previously defined or disclosed in the Specification while it is not a well-known technical term in the computer art. Therefore, claim 22 is failing to particularly point out the subject matter being claim in the invention.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 5, and 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Nickolls et al. (US Patent 5,243,699).

As per claim 1, Nickolls et al. discloses a method for double buffering serial transfers during a write operation (See Fig. 8), comprising:

(a) serially transferring address bits of a word into an address shift register (see claim 10, lines 48-50, wherein the address shift register engaged in the serial transfer; and see col. 2, lines 14-15, wherein the I/O data is a word),

(b) serially transferring data bits of the word into a data shift register (see claim 10, lines 58-60);

(c) after completing the serial transfer of the address bits into the address shift register, transferring, in parallel, the address bits into an address holding register (see claim 10, lines 50-55, wherein the address parallel register is equivalent to address holding register); and

(d) after completing the serial transfer of the data bits into the data shift register, transferring, in parallel, the data bits into a data holding register (see claim 10, lines 50-64);

wherein after completing the parallel transfer of the address bits and data bits from the address and data shift registers to the address and data holding registers, the address and data shift registers are available to serially receive additional address bits and data bits of an additional word (wherein the shift registers are available to serially receive additional bits of data is an inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is designed to transfer plurality of data items between the processor and the I/O device, see claim 1, preamble).

The description of the specification on col. 8, line 60 – col. 9, line 25 contains additional information that is relevant to the cited claim 10 above.

As per claim 2, Nickolls et al. a method wherein:

step (a) include serially transferring one of the address bits per clock cycle is an inherent feature in the system of Nickolls et al. since serial transfer is performing one bit of data per clock cycle;

step (b) include serially transferring one of the data bits per clock cycle is an inherent feature of Nickolls et al. since serial transfer is performing one bit of data per clock cycle;

step (c) includes transferring, in parallel, the address bits into the address holding register in one clock cycle or less (see col. 3, lines 47-51, wherein the data is transferred from the serial portion to parallel portion in one cycle, wherein the registers include address register); and

step (d) includes transferring, in parallel, the data bits into the data holding register in one clock cycle or less (see col. 3, lines 47-51, wherein the data is transferred from the serial portion to parallel portion in one cycle, wherein the registers include data register).

As per claim 5, Nickolls et al. discloses a method wherein steps (c) and (d) are performed simultaneously. See col. 12, lines 61-65, wherein the address and data are transferred to the parallel registers.

As per claim 7, Nickolls et al. discloses a method, wherein the word is received over a serial line from a host. See col. 2, lines 14-16.

As per claim 8, Nickolls et al. discloses a method wherein the transferring of the address bits and the data bits to the address and data holding registers in steps (c) and (d) is over parallel lines. See claim 10, lines 58-64.

As per claim 9, Nickolls et al. discloses a method wherein the address bits specify a location to which to write the data bits. See col. 2, lines 22-25.

As per claim 10, Nickolls et al. discloses a method for double buffering serial transfers during a read operation (See Fig. 9) in which a host attempts to read data from a location in a device, comprising:

(a) serially transferring address bits received from the host into an address shift register in the device (See claim 10, lines 48-50 and the communication is between the processor/host with the I/O device as disclosed in col. 1, lines 31-34),

(b) serially transferring data bits present in a data shift register in the device, from the device to the host, wherein the data bits present in the data shift register are associated with a previous read operation (see claim 10, lines 58-60, wherein it is readily apparent that the data is associated with the address given in the previous operation);

(c) after completing the serial transfer of the address bits into the address shift register, transferring, in parallel, the address bits into an address holding register in the device, wherein the address bits identify the location, which contains requested data bits (see claim 10, lines 50-56); and

(d) after the requested data bits are read from the location into a data holding register, transferring the requested data bits, in parallel, from the data holding register to the data shift register (see claim 10, lines 62-64);

wherein the requested data bits will be transferred, serially, from the data shift register to the host the next time the host performs a read operation (See col. 2, lines 21-25 and lines 34-38).

The description of the specification on col. 8, line 60 – col. 9, line 25 contains additional information that is relevant to the cited claim 10 above.

As per claim 11, Nickolls et al. discloses a double buffering system for use in a device to which a host writes data (see Fig. 8), and from which the host reads data (see Fig. 9), comprising:

an address shift register to serially receive address bits from a host, the address bits identifying a location to which to write data bits, or from which to read data bits (see claim 10, lines 48-52);

a data shift register, to serially receive data from the host during a write operation, and to serially transfer data to the host during a read operation (claim 10, lines 58-61);

an address holding register/address parallel register to receive a parallel transfer of address bits from the address shift register (see claim 10, lines 53-56); and

a data holding register/data parallel register, to receive a parallel transfer of data bits from the data shift register during a write operation, and to transfer in parallel data bits to the data shift register during a read operation (see claim 10, lines 62-64).

The description of the specification on col. 8, line 60 – col. 9, line 25 contains additional information that is relevant to the cited claim 10 above.

As per claim 12, Nickolls et al. discloses a system wherein during a write operation, after the parallel transfers of the address bits and data bits from the address and data shift registers to the address and data holding registers, the address and data shift registers are available to serially receive additional address bits and data bits from the host (See claim 1, preamble, wherein the shift registers are available to serially receive additional bits from the host is an inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is designed to transfer plurality of data items between the processor and the I/O device).

As per claim 13, *it is an inherent feature in Nickolls et al. that* during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation since the address is required in order for the system to specifically retrieved the requested data since a read operation is supposed to retrieve the data that is requested, which is corresponding to the data address provided. This rejection can further be enforced by the disclosure on col. 2, lines 21-25 of Nickolls et al.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699).

As per claim 3, although Nickolls et al. did not specifically teach wherein the parallel transfer the address bits in step (c) is performed before the serial transfer of the data bits in step (b) is completed.

However, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to implement the system so that the address bits are parallel transferred before the serial transfer of the data bits. The motivation of doing so is to enable the system to receive the address before the data arrives at the destination. In doing so, the location that data to be stored can be located before the data arrives and efficiently store the data into said location once the data arrives since the address location has already located.

As per claim 4, although Nickolls et al. did not specifically teaches wherein step (c) is performed before step (d).

However, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant invention to recognize that it is user design choice to modify the system of Nickolls et al. to perform the step (c) before the (d) so that the address that defines the location of the data to be written is transferred to the destination before the data arrives. The motivation of doing so is to enable the system to locate and efficiently store the data into the destination location once the data arrives since the address has already decoded or located.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) in view of Tomishima et al. (US Patent 6,470,467).

As per claim 6, Nickolls et al. did not particularly teach the address and data holding registers each comprises a latch.

Tomishima et al. discloses a latch (Fig. 2, item 1049 and 1073b) to latch the address and the data.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the holding registers of Nickolls et al. as a latch in order to stage the data and the address before swapping as disclosed in cited claim 10 of the Nickolls et al. The motivation of doing so is enable a device/register to latch/store the data before transferring to the next destination.

8. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) in view of Ku et al. (US Patent 5,812,881).

As per claim 14, Nickolls et al. did not specifically disclose a serial controller to determine, based on a mode bit, whether a serial transfer from the host to the device is associated with a read operation or a write operation.

However, Ku et al. discloses a method of determining whether the operation is a read or a write operation (see col. 3, lines 38-42, wherein the mode bit is inherent feature in Ku et al. in digital logic art).

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Ku et al. with the method of Nickolls et al. in order to arrive at the current invention. The motivation of doing so is to enable the system of Nickolls et al. to efficiently determine a correct mode of operation in order to either transfer or retrieve data to or from the holding register.

As per claim 16, the serial controller includes a switch to select between transferring bits to the first shift register and the second shift register is a readily apparent feature in the system of Nickolls et al. since the system of Nickolls et al. is having a data shift register and an address shift register, which two of them are separated from each other. Therefore, there has to be a switch in order to assign the address bits to the address shift register and the data bits to the data shift register.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) and Ku et al. (US Patent 5,812,881) in view of Dunki-Jacobs (US Patent 4,641,276).

As per claim 15, Nickolls et al. discloses a wherein the serial controller (Fig. 6, item 520) includes a byte counter (Fig. 6, item 530) that receives a control signal (513), and wherein the counter functions as an incrementer or as a shift register to determine which byte of the registers is to be accessed by the decoder array 529.

Nickolls et al. and Ku et al. did not particularly teach a counter that which bits are address bits and which bits are data bits. However, Dunki-Jacobs discloses a counter that determines the address bits and the data bits to appropriately transferred to the data path. See col. 6, lines 17-29.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method teaches by Dunk-Jacobs with the method of Nickolls et al. in order to arrive at the current invention. The motivation of doing so is to assign the data bit in a word correctly to the corresponding data shift register (Fig. 6, item 524 of Nickolls et al.) and address shift register (Fig. 6, item 544) in order to avoid any error or delay if the system is wrongly transferring the data bits.

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) in view of Gushima et al. (US Patent 5,506,825).

As per claim 17, Nickolls et al. discloses a system comprising:

an address shift register to serially receive address bits from a host, the address bits identifying a location to which to write data bits, or from which to read data bits (see claim 10, lines 48-52);

a data shift register, to serially receive data from the host during a write operation, and to serially transfer data to the host during a read operation (claim 10, lines 58-61);

an address holding register/address parallel register to receive a parallel transfer of address bits from the address shift register (see claim 10, lines 53-56); and

a data holding register/data parallel register, to receive a parallel transfer of data bits from the data shift register during a write operation, and to transfer in parallel data bits to the data shift register during a read operation (see claim 10, lines 62-64).

an address shift register to serially receive address bits from a host, the address bits identifying a location to which to write data bits, or from which to read data bits;

a data shift register, to serially receive data bit from the host during a write operation, and to serially transfer data bits to the host during a read operation,

an address holding register to receive a parallel transfer of address bits from the address shift register; and

a data holding register, to receive a parallel transfer of data bits from the data shift register during a write operation, and to transfer in parallel data bits to the data shift register during a read operation.

Nickolls et al. teaches a serial controller (Fig. 6, item 520) to control serial transfers between the I/O device (Fig. 1, item 80) and a host (Fig. 1, item 10).

Nickolls et al. did not particularly teach a laser driver. However, Gushima et al. discloses a laser driver (Fig. 13, item 48, col. 15, lines 1-3) as an I/O device to receive and transfer the data from the host. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the I/O device of Nickolls et al. to become a laser driver as disclosed by Gushima et al. in order to arrive at the current invention. The motivation of doing so is to utilize the efficient data transferring method/system of Nickolls et al. to assist with the data transferring between the host and the laser driver in order to improve the system reliability and data throughput.

As per claim 18, Nickolls et al. teaches a system wherein during a write operation, after the parallel transfers of the address bits and data bits from the address and data shift registers to the address and data holding registers, the address and data shift registers are available to serially receive additional address bits and data bits from the host. See claim 1, preamble, wherein the shift registers are available to serially receive additional bits from the host is an inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is designed to transfer plurality of data items between the processor and the I/O device.

As per claim 19, *it is readily apparent feature in Nickolls et al. that* during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation since the address is required in order for the

system to specifically retrieved the requested data since a read operation is supposed to retrieve the data that is requested, which is corresponding to the data address provided. This rejection can further be enforced by the disclosure on col. 2, lines 21-25 of Nickolls et al.

As per claim 22, Nickolls et al. discloses a system further comprising:

a parallel address bus (Fig. 6, item 518) connecting the address holding register (Fig. 6, item 540) to a register bank (Fig. 6, item 540); and

a parallel data bus (Fig. 6, item 516) connecting the data holding register (Fig. 6, item 520) to the register bank (Fig. 6, item 540).

As per claim 23, the timing memory that connects to the parallel address bus and parallel data bus is an inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is requiring a pipelined message transmission time to transmit the data between the source and the destination. Therefore, a timing device/memory has to exist in the system of Nickolls et al. in order to assist the data and address to be transferred along the parallel buses at a correct timing.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) and Gushima et al. (US Patent 5,506,825) in view of Dunki-Jacobs (US Patent 4,641,276).

As per claim 20, Nickolls et al. discloses a wherein the serial controller (Fig. 6, item 520) includes a byte counter (Fig. 6, item 530) that receives a control signal (513), and wherein the counter functions as an incrementer or as a shift register to determine which byte of the registers is to be accessed by the decoder array 529.

Nickolls et al. did not particularly teach a counter that which bits are address bits and which bits are data bits. However, Dunki-Jacobs discloses a counter that determines the address bits and the data bits to appropriately transferred to the data path. See col. 6, lines 17-29.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method teaches by Dunk-Jacobs with the method of Nickolls et al. in order to arrive at the current invention. The motivation of doing so is to assign the data bit in a word correctly to the corresponding data shift register (Fig. 6, item 524 of Nickolls et al.) and address shift register (Fig. 6, item 544).

As per claim 21, the serial controller includes a switch to select between transferring bits to the first shift register and the second shift register is in inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is having a data shift register and an address shift register, which two of them are separated from each other. Therefore, there has to be a switch in order to assign the address bits to the address shift register and the data bits to the data shift register.

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) and Gushima et al. (US Patent 5,506,825) in view of Toshima et al. (US Patent 6,470,467).

As per claim 24, Nickolls et al. did not particularly teach the address and data holding registers each comprises a latch.

Tomishima et al. discloses a latch (Fig. 2, item 1049 and 1073b) to latch the address and the data.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the holding registers of Nickolls et al. as a latch in order to stage the data and address before swapping as disclosed in claim 10 of the Nickolls et al. since a latch is well know to one having an ordinary skill in the art as a device/register to latch/store the data before transferring to the next destination.

***Allowable Subject Matter***

12. Claims 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thanh D. Vo
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AU 2189
8/17/2006

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